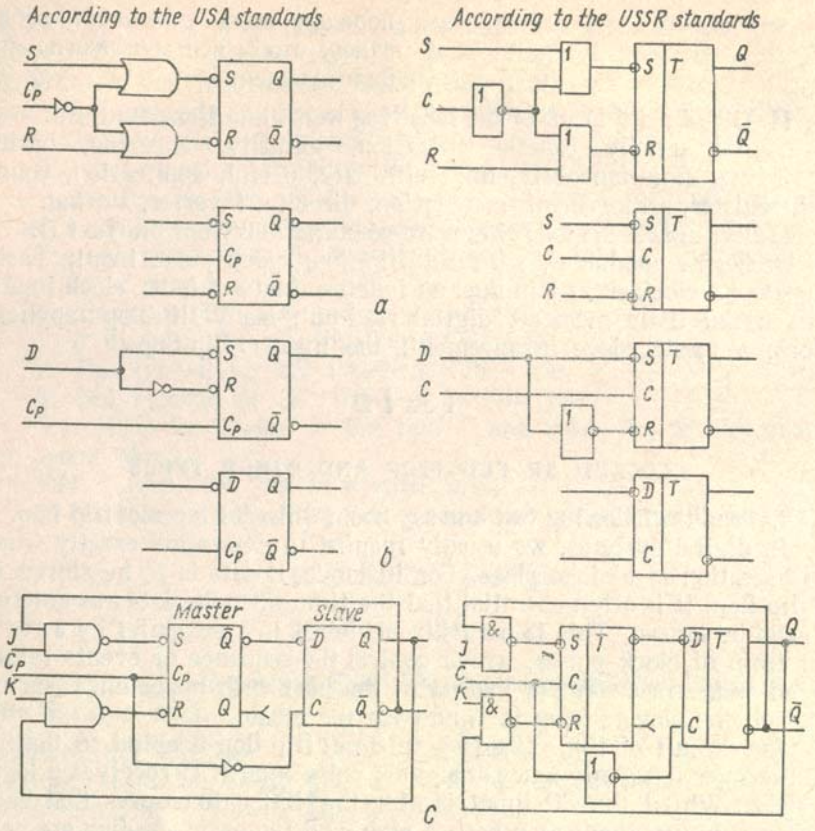

Fig. 3.9. Logic-circuit diagrams and symbols:
a for a clocked SR flip-flop; *b* for D-type flip-flop; *c* for clocked JK flip-flop master-slave type.

during that period. This is accomplished by using two flip-flops together in a master-slave arrangement. The master flip-flop responds to data from the input whilst the clock is high, but this is only passed on to the slave (output) flip-flop as the clock goes back to zero. One such arrangement is shown in Fig. 3.9*c*.

The two inputs are by convention labelled *J* and *K*. A clocked SR flip-flop on the left acts as the master, whilst the *D* flip-flop on the right acts as the slave. Note the clock input goes directly to the master flip-flop but via an inverter to the slave. This means that whilst the clock input is low, the slave is receiving a logic 1 at its CP input and the *Q* output is ready to respond to any change in the *D* input. There cannot, however, be any change here whilst the clock is low, because the master flip flop is locked, storing whatever input it had when the clock was last high.

I. a) Skim through the Text D and divide it into logical parts. b) Choose the key sentences and translate them.

II. Find the part of the text describing application of flip-flop.

III. Answer the following questions embracing the contents of the Text D.

1. What is essential if data is to be stored in a flip-flop? 2. How is this normally achieved? 3. What does Fig. 3.9*c* show? 4. When can SR flip-flop change state? 5. What does the NOT gate ensure whilst the CP input is at 0? 6. What is the *D*, or data, flip-flop? 7. What application does the useful little memory of flip-flop find? 8. What does the master flip-flop respond to?

IV. Ask additional questions on the Text D.

V. Discuss the problem of different types of flip-flops.

VI. Examine Fig. 3.9 and comment on:

1. For a clocked SR flip-flop.
2. For *D*-type flip-flop.
3. For clocked JK flip-flop master-slave type.

VII. Make up a plan of the Text D and give a short summary of it.

VIII. Look through the latest magazines and find additional information on flip-flops. Discuss it.

III. GRAMMAR EXERCISES

I. Pay attention to the Perfect Passive forms while translating these sentences.

1. In all the logic circuits that have so far been described, at any point in time the output has been directly related to the input by some logic combination, except for some short propagation delay. 2. Simple digital gates NOR, NAND, etc. have been described in the previous lessons.

II. Put questions to the words in bold type.

1. **In digital system,** we usually require to determine exactly when an operation is to take place. 2. **The clocked SR flip-flop** can only respond to the *R* and *S* inputs during a logic 1 clock pulse. 3. The output is held **until the clock input goes from 0 to 1.** 4. This is accomplished using two flip-flops together **in a master-slave arrangements.** 5. The two inputs are by convention **labelled *J* and *K*.**

III. Define the tense-forms in the Passive Voice and translate the sentences with them.

1. Combinational circuits are also known as non-regenerative circuits. 2. Q_1 is reverse-biased to cutoff. 3. The techniques described in 2 to 4 are widely used to change the operating of a flip-flop. 4. Small capacitors are often connected across the *R* resistors in Fig. 3.6*a* and 3.6*b*. 5. Transient response of the circuit is improved considerably by use of the above speedup capacitors. 6. Cross-coupled single-input

NOR stages are used in the above flip-flop circuit. 7. Symbols for the OR and NOT (invert) operations are indicated in the figure. 8. If the input signal on the set line is reduced to ground potential, the flip-flop continue to store a 1. 9. This last state is maintained when the reset line is grounded.

IV. Pay attention to modal verbs with the Passive Infinitive while translating these sentences.

1. The above circuit may be analysed by redrawing it as in Fig.3.6*b*. 2. Flip-flop stages can also be constructed with AND-NOT logic as shown in the diagram of Fig. 3.7*b*. 3. This circuit configuration can be implemented by cross-coupling single-input DTL NAND gates. 4. Because the present flip-flop configuration can be set to 1 and reset to 0, the circuit is generally referred to as a "set-reset" (SR) flip-flop.

V. Define the forms and functions of the Infinitive in the following sentences and translate them.

1. The stage is considered to be a NAND-type flip-flop. 2. The circuit is now considered to be storing a 1. 3. The output lines are shown to have the binary values associated with the storage of a 1. 4. If data is to be stored in a flip-flop, it is often essential that the time when the data was entered should be known. 5. The output must be held steady long enough to be read.

VI. Define the forms and functions of the Participle in these sentences and translate them.

1. Fig. 3.7*c* shows a flip-flop having two input-signal lines. 2. The *D*, or data, flip-flop is a clocked RS flip-flop operated from just one input. 3. This is normally achieved in a computer by a regular train of clock pulses, which control the sequence of events rather as an orchestra conductor maintains the best with his baton ensuring that all the players keep in time with the music.

Lesson 5. CONTROL IN A COMPUTER

I. INDEPENDENT WORK

In the Laboratory

1. Skimming Reading

PRE-TEXT EXERCISES

I. a) Listen and repeat after the speaker. b) Practise the pronunciation of the following.

I. [ou] road, load, foam; [oi] oil, point, alloy; [u] book, look, took, through; [u:] tool, food, root; [ɔ:] door, floor, thought, coarse, source, store, perform; [au] out, output, outgrowth, allow, however; [a:] heart, hard, class; [ei] main, obtain.

II. Approximately [ə'prɔksimitli], subsequent ['sʌbsikwənt], sequential [si'kwenʃəl], consecutive [kən'sekjutiv], synchronize ['siŋkrənaiz].

II. a) Make sure that you know these words. Say what Russian words help you to guess their meanings. b) Repeat these words after the speaker.

Functional, machine, minimize, generated, structure, equivalent, categories, function, identify, unique, instruction, decode, data, signal, activity, elementary, action, typically.

III. a) Listen, repeat and memorize the following words and word-combinations. b) Check if you know the meaning of these words.

Hardware аппаратура, аппаратное обеспечение; in hardware схемно (с помощью схем, аппаратуры); outgrowth продукт; the heart of the system основа, основной узел системы; implementation осуществление, выполнение; execute выполнять; interprete переводить.

IV. a) Find and learn the following terms from the Text A and the Text B. b) Translate the sentences with them.

A general purpose CPU универсальный центральный процессор; memory facility устройство памяти; I/0 section устройство ввода / вывода; main memory основная память; conventional or random logic обычная или случайная логика; programmable logic array программируемая (перестраиваемая) логическая матрица; microprogram control микропрограммное управление; instruction decode расшифровка команды; operand fetch выборка операнда; logic gates логические вентили; instruction execute выполнение команды; instruction fetch выборка команды (из ЗУ); inctruction set набор команд; data fetch выборка данных; address modification logic логические схемы модификации адреса; stored instruction хранимая (в памяти) команда; the descrete component era эра дискретных компонентов; the LSI (large scale integration) approach to random logic подход к построению произвольной логики на больших микросхемах; common control sequence общая управляющая последовательность; to share the same hardware использовать то же оборудование; flow of instructions поток команд.

V. Analyse the following words from the viewpoint of their structure.

Microprogram, outgrowth, irregular, hardware, throughout, well-organized, relationship.

VI. Give English equivalents to the Russian words in brackets and translate the sentences into Russian.

1. (Применение) of the instruction set, which is unique to each design, (определять) the control section of the machine. 2. (Количество) operand fetches (зависеть) on the instruction set. 3. Since each (команда) performs a unique function, the control sequence (отличаться) from instruction to instruction. 4. Fig. 3.10*a* (показывать) the relationship of basic control (функции). 5. The address modification (применяться) to both operand and instruction fetches. 6. Fig. 3.10*b* illustrates (поток данных) of instruction from the main (память). 7. The address modification logic for program (или данные) normally (разделять) the ALU hardware.

Text A

A CONTROL SECTION IN THE COMPUTER

I. a) Listen to the text, mind the English intonation. b) Read the text to yourself and grasp the main idea of it.

A general purpose CPU may be considered as being divided into four function units: a control section, a memory facility, an arithmetic logic unit (ALU), and I/0 section. The control section is the heart of the system; it interprets and executed stored instructions from main memory. The implementation of the instruction set, which is unique to each design, defines the control section of the machine.

Three techniques are used to implement the control section in hardware: conventional or random logic, programmable logic array (PLA), and microprogram control. Random logic is an outgrowth of the descrete component era; logic gates are minimized to reduce the hardware cost. This gave rise to an irregular structure; control signals are scattered throughout the entire machine in an apparently random manner. An LSI approach to random logic is the PLA. The logic structures generated by random logic and the PLA's are equivalent.

Control operations may be classified into four basic categories: instruction fetch, instruction decode, operand fetch, and instruction execute. These operations dictate the necessary control signals required to implement the control functions defined by the instruction set of a computing machine.

The instruction fetch operation, which provide the control linkage from instruction to instruction, allows a continuous flow of instructions to be executed. The decode function identifies the various classes of instructions that have common control sequence. This permits different instructions with identical operations to share the same hardware. A data fetch (commonly referred to as an operand fetch) is required to obtain the prescribed data from memory. The number of operand fetches depends on the instruction set.

2. Average Reading

Text B

CONTROL SIGNALS

I. a) Listen to the text. b) Read it (time limit is 3 min.). c) Find the part of the text dealing with the relationship of basic control functions. Translate it.

To implement an instruction, various control signals are required to coordinate the activities occurring at different times. Each action is an elementary operation and, by itself, may not accomplish the desired result. However, the "orchestration" of the various actions into a well-organized sequence results in the operation specified by the instruction. The number of control signals for a given instruction depends on its complexity and the internal structure of the machine. Since each instruction performs a unique function, the control sequences differ from instruction to instruction.

Fig. 3.10*a* shows the relationship of basic control functions. They implement not only the execution of instructions but also perform the addressing of sequencing from instruction to instruction to form a program sequence. The address modification applies to both operand and instruction fetches. Many ways of altering an instruction sequence or performing a data fetch illustrate the strength and flexibility provided by a stored program. Fig. 3.10*b* illustrates the flow of data of instruction from the main memory The address modification logic for program or data normally shares the ALU hardware indexing operations are to be performed under the control of the execution logic.

ASSIGNMENTS

I. Choose the key sentenses from the text A and compare them with the title of the text. b) Say what the text is about.

II. a) Skim through the Text B and find the part of it dealing with the number of control signals for a given instruction. b) Discuss it with your fellow-student.

III. a) Find the part of the Text B containing information about ways of altering an instruction sequence. b) Make a short written summary about it.

IV. Answer the following questions embracing the contents of the texts.

1. How may a general purpose computer be considered? 2. What function units has a general purpose CPU? 3. What is the function of the control section? 4. What does the implementation of the instruction set define? 5. What techniques are used to implement the control section in hardware? 6. What four basic categories may control operation be classified into? 7. What does the instruction fetch operation allow? 8. What is required to obtain the prescribed data from memory? 9. What does the number of operand fetches depend on? 10. What are required to coordinate the activities occurring at different times? 11. What does the number of control signals for a given instruction

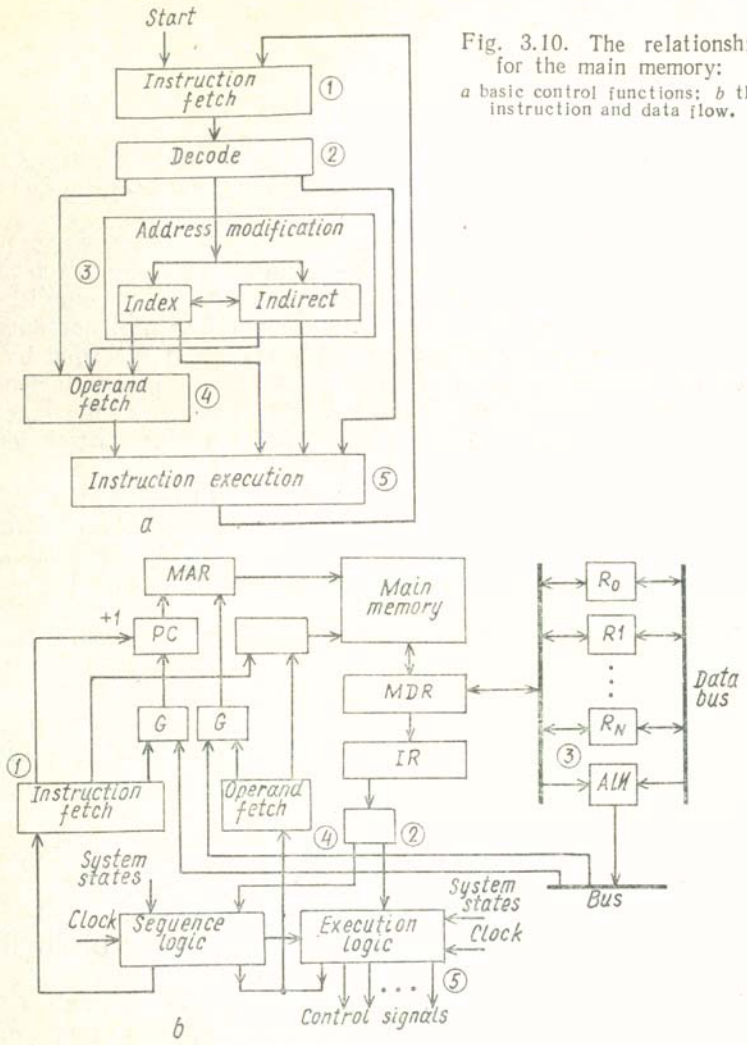

Fig. 3.10. The relationship for the main memory:
a basic control functions; *b* the instruction and data flow.

depend on? 12. What does Fig. 3.10*a* show? 13. What do the basic control functions implement? 14. To what does the address modification apply? 15. What figure illustrates the flow of data of instruction from the main memory?

V. Examine Fig. 3.10 and comment on:

1. Basic control functions.
2. The instruction and data flow.

VI. Speak on:

1. Control operations.
2. Functional units of a general purpose CPU.

VII. Make a short written summary of the Text B.

II. CLASSWORK

3. Close Reading

PRE-TEXT EXERCISES

I. Be sure that you know these words.

Approximately приблизительно; destroy разрушать; restore восстанавливать; nearly приблизительно; imply значить, подразумевать; coincide совпадать; realize осуществляться; correspond соответствовать; sequential последовательный, являющийся продолжением; consecutive последовательный.

II. Find these word-combinations and terms in the Text C and translate sentences with them.

Execution circuitry исполнительные схемы; the memory cycle цикл (работы) памяти; machine cycle time длительность машинного цикла; the access time время обращения; core memory system система памяти (ЗУ) на магнитных сердечниках; sense v. считывать; in the range в диапазоне; either destroyed or cleared либо разрушается, либо стирается; subsequent read interval последующий интервал считывания; instruction-execution rate скорость выполнения команды; maximum data transfer rate максимальная скорость передачи данных; the overlap operation перекрывающиеся операции; clock pulses тактовые импульсы; semiconductor memory полупроводниковая память; nondestructive operation операция без разрушения информации; in consecutive order в последовательном порядке; incremented by one count с приращением на единицу; each time каждый раз; program counter (PC) счетчик команд; the entry point точка ввода, входная точка.

Text C

CORE MEMORY CYCLE

I. a) Read the Text. b) Find the part of it describing a timing sequence of simple instructions.

Typically, a core memory cycle is divided into two approximately equal intervals: a read operation and a write operation (see Fig. 3.11*a*). The read interval represents the operation time required by the memory to decode the address, switch the cores, and sense the outputs before the data are presented to the CPU. This interval is defined as the access time. As the information stored in memory at that address is read from the cores, it is either destroyed or cleared. To restore the data, the information must then be written back into the cores immediately following the read interval. With a cycle time in the range of 1 to several microseconds, nearly all control operations required by the instruction can be completed during the write interval and subsequent read interval. This implies that the memory access rather than the control operations is the limiting factor in the instruction

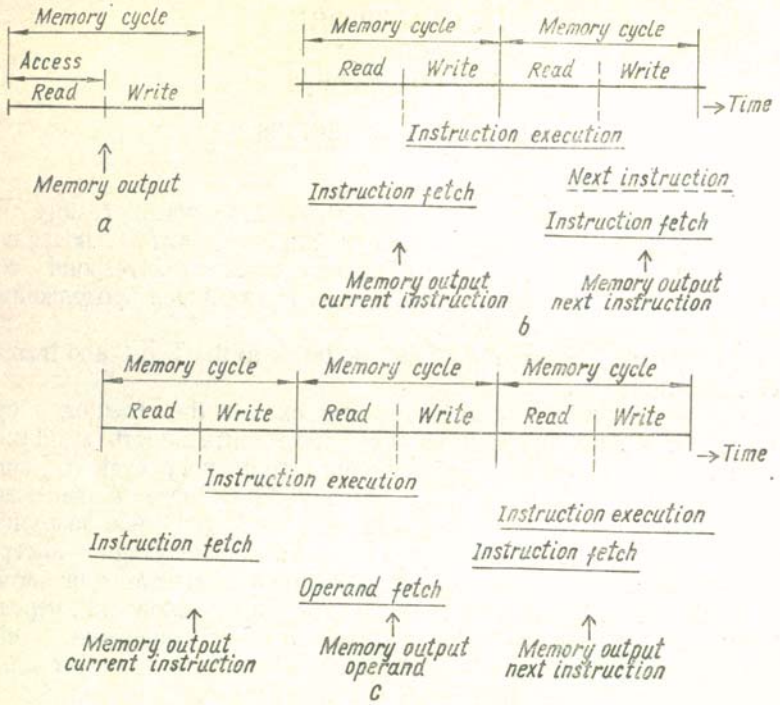

Fig. 3.11. The memory fetch operation:
a memory cycle; *b* instruction cycle; *c* instruction cycle with operand fetch.

execution rate of a processor. However, this is not true for more complicated instruction, such as multiplication or division. These instructions require many cycles of repeated operations without any memory access.

By organizing the basic cycle to coincide with the memory cycle, the maximum data transfer rate between main storage and the processor may be realized. Fig. 3.11*b* shows a timing sequence of simple instructions that can be fully implemented during the write and read intervals. The overlap operations of instruction fetch and execution keep the memory access rate at the 100 per cent level. Fig. 3.11*c* shows an instruction requiring an operand fetch. In both cases, the memory access and the instruction execution are completely synchronized to use the memory at its fastest possible rate.

A program sequence is normally executed in consecutive order with the program address incremented by one count each time an instruction is fetched from memory. At times, it is necessary to branch from the regular program sequence and jump to a new one. The address of the next instruction found in the program counter (PC) will be changed to correspond to the entry point of the new program sequence. Fig. 3.12*a* and 3.12*b*, respectively, show the hardware and the timing chart of a sequential instruction fetch. The PC is automatically incre-

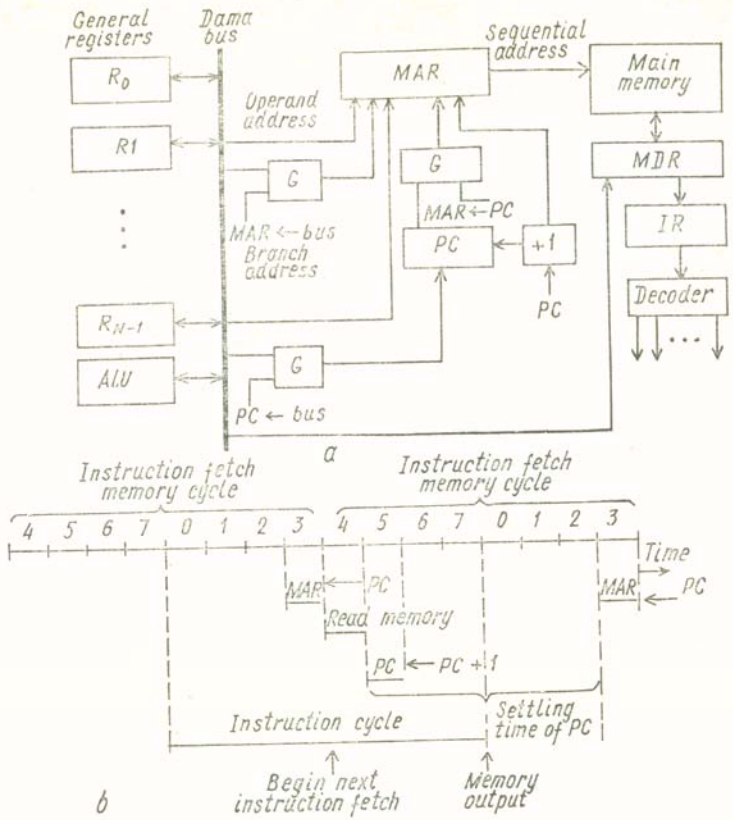

Fig. 3.12. Memory addressing:
a functional diagram; *b* timing sequence of simple sequential addressing.

mented by one count after its content is transferred to the memory address register (MAR). A serial counter rather than a high speed parallel binary counter can be used in the implementation of the PC, since the count does not have to be settled until the next PC-to MAR transfer.

ASSIGNMENTS

I. a) Skim through the Text C and divide it into logical parts. b) Choose the key sentences from the text and translate them.

II. Find the part of the Text C containing information about the maximum data transfer rate between main storage and the processor. Discuss it.

III. Answer the following questions embracing the contents of the Text C.

1. What does instruction sequencing provide? 2. How many intervals is a core memory cycle divided into? 3. What does the read inter-

val represent? 4. How is this interval defined? 5. What happens to the information stored in the memory when it is read? 6. What is necessary to restore the data? 7. What is the limiting factor in the instruction executive rate of a processor? 8. How may the maximum data transfer rate between main storage and the processor be realized? 9. What does Fig. 3.12*b* show? 10. What figure shows an instruction requiring an operand fetch?

IV. Ask additional questions on the contents of the Text. C.

V. Discuss the problem of core memory cycle.

VI. Examine Fig. 3.12 and comment on:

1. Functional diagram.
2. Timing sequence of simple sequential addressing.

VII. Prepare a dialogue on your own situation.

VIII. Speak on the text according to your own plan.

IX. Express your opinion of the text from the viewpoint of your speciality.

X. Make a short summary of the text.

XI. Translate the Text C to be sure you understand it well.

4. Searching Reading

PRE-TEXT EXERCISES

I. Match the following English words and word-combinations with the Russian ones.

saturate	относиться
subsequent	требовать
refer	общая точка
certain features	насыщать
require	повышать(ся)
rise	обычно
common point	сопротивление нагрузки
typically	последующий
load resistor	определенные черты

II. Find the following word-combinations in the Text D and translate the sentences with them.

Subsequent forms of logic circuits; forward base current; direct-coupled transistor logic; transistor logic circuit; a succeeding stage; DCTL configuration; latter transistor; collector-current cutoff; fan-out transistor; supply voltage; base-input resistor.

Text D

DIRECT-COUPLED TRANSISTOR LOGIC

I. a) Read the following text and say about transistor logic. b) Review the text.

In one of the early forms of transistor logic circuit, the collector of an inverter transistor was connected directly to the base of a succe-

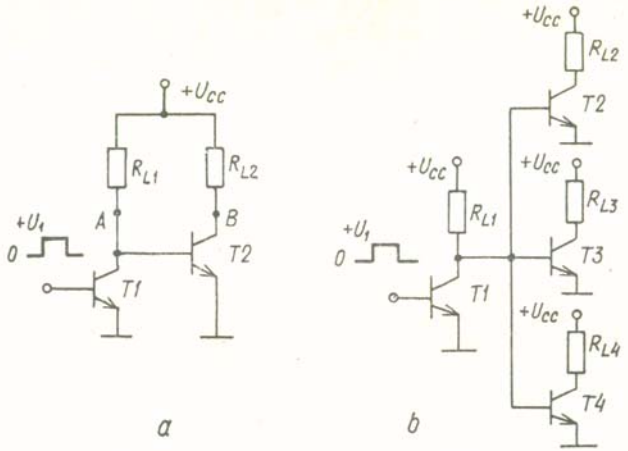

Fig. 3.13. Logic circuits of DCTL-type:
a a simple two-transistor circuit with one input; *b* fan-out loading of a DCTL inverter.

eding stage. This form of transistor logic is referred to as "direct-coupled transistor logic" (DCTL). Although the DCTL configuration is not widely used today, it is discussed here in order to illustrate certain features of subsequent forms of logic circuits.

Fig. 3.13 shows a DCTL circuit. Consider, for the moment, that the base of transistor T_2 is not connected to the collector of transistor T_1 and also that this latter transistor is at collector-current cutoff; collector voltage of T_1 is close to the U_{CC} level. If the base of T_2 is now connected to the collector of T_1 current will flow through R_{L1} into the base of T_2 and the voltage at point A will fall to the $U_{BE(ON)}$ level of T_2. Forward base current to T_2 saturates this device, and the voltage at point B is close to ground potential. When T_1 is driven to saturation, the voltage at point A becomes equal to the $U_{CE(sat)}$ level of T_1. If this voltage is less than that required to turn on T_2, the voltage at point B will rise to nearly the level of U_{CC}.

The bases of two or more transistors can be driven from a common point, as shown in Fig. 3.13. Each of these fan-out transistors can be connected, at their collectors, to bases of other transistors.

Only one supply voltage is normally used for DCTL circuitry. This voltage is typically 1.5 to 5 volts. In the circuit of Fig. 3.13 R_{L1} serves as a load resistor for T_1 and is also the base-input resistor to T_2, T_3 and T_4.

ASSIGNMENTS

I. Answer the following questions embracing the contents of the text.

1. Where was the collector of an inverter transistor connected directly to the base of a succeeding stage? 2. What is referred to as "direct-coupled transistor logic"? 3. Is the DCTL configuration widely

used today? 4. What does Fig. 3.13 show? 5. When will current flow through R_{L1} into the base of T_2? 6. When does the voltage at point A become equal to the $U_{CE(sat)}$ level of T_1? 7. Where can the bases of two or more transistors be driven from? 8. What can each of these fan-out transistors be connected to? 9. What voltage is normally used for DCTL circuitry?

II. Express your opinion of DCTL.

III. Discuss the problem of transistor logic.

IV. Examine Fig. 3.13 and comment on:

1. A simple two-transistor circuit with one input.
2. Fan-out loading of a DCTL inverter.

V. Make a short summary of the Text D.

VI. Translate the following sentences into English without using the dictionary.

1. Универсальный центральный процессор делится на 4 функциональных блока. 2. Устройство управления является основой системы для интерпретирования и выполнения хранимых команд, выбранных из основной памяти. 3. Работа с выборкой команд делает возможным выполнять команды непрерывным потоком. 4. Команды должны выполняться непрерывным потоком. 5. Количество выборов операндов зависит от семейства (набора) команд. 6. Требуются различные сигналы управления, чтобы скоординировать работу в различные моменты времени.

VII. Look through the latest magazines and find additional material on transistor logic for summary and discussion.

III. GRAMMAR EXERCISES

I. Translate these sentences. Pay attention to the modal verbs with the Passive Infinitive.

1. A general purpose CPU may be considered as being devided into four functional units. 2. Control operations may be classified into four basic categories. 3. To restore the data, the information must then be written back into the cores immediately following the read interval. 4. With a cycle time in the range of 1 to several microseconds, nearly all control operations required by the instruction can be completed during the write interval and subsequent read interval. 5. Fig. 3.11*b* shows a timing sequence of simple instructions that can be fully implemented during the write and read intervals.

II. Find the Infinitives in the following sentences. Define their functions and translate the sentences.

1. Three techniques are used to implement the control section in hardware. 2. Logic gates are minimized to reduce the hardware cost. 3. The instruction fetch operation allows a continuous flow of instructions to be executed. 4. A data fetch is required to obtain the prescribed data from memory. 5. To implement an instruction various control signals are required to coordinate the activities occurring at different times. 6. A serial counter rather than a high speed parallel binary counter can be used in the implementation of the PC, since

the count does not have to be settled until the next PC-to MAR transfer.

III. Define the function of the Participles in the following sentenses and translate them.

1. The logic structures generated by random logic and the PLA's are equivalent. 2. These operations dictate the necessary control signals required to implement the control functions defined by the instruction set of a computing machine. 3. As the information stored in memory at that address is read from the cores, it is either destroyed, or cleared. 4. Fig. 3.11*c* shows an instruction requiring an operand fetch. 5. In one of the early forms of transistor logic circuit, the collector of an inverter transistor was connected directly to the base of a succeeding stage.

IV. Translate the following sentences paying attention to the verbs in the Passive Voice.

1. Control signals are scattered throughout the entire machine in an apparently random manner. 2. A core memory cycle is divided into two approximately equal intervals. 3. The memory access and the instruction execution are completely synchronized to use the memory at its fastest possible rate. 4. The address of the new instruction found in the program counter (PC) will be changed to correspond to the entry point of the new program sequence. 5. The PC is automatically incremented by one counter after its content is transferred to the memory address register (MAR).

V. Put questions to the words in bold type.

1. This **permits different instructions** with identical operations **to share the same hardware.** 2. **The number of operand fetches** depends **on the instruction set.** 3. The read interval **is defined as the access time.** 4. These instructions **require** many cycle of **repeated operations without any memory access.** 5. **It** is necessary to branch **from the regular program sequence** and jump to a new one.

Chapter IV. RADIO ELECTRIC CIRCUITS AND MEASURING TECHNIQUE

Lesson 1. NEGATIVE FEEDBACK

I. Independent Work.
In the Laboratory:
1. *Skimming Reading.*
Pre-text Exercises.
Text A. Frequency Response.
2. *Average Reading.*
Text B. Equation for an Amplifier with Feedback.
Assignments.
II. Classwork.
3. *Close Reading.*
Pre-text Exercises.
Text C. Non-linear Distortion.
Assignments.
4. *Searching Reading.*
Pre-text Exercises.
Text D. Input and Output Impedance.
Assignments.
III. Grammar Exercises.

I. INDEPENDENT WORK

In the Laboratory

1. Skimming Reading

PRE-TEXT EXERCISES

I. Make sure that you know these words. b) Say what Russian words help you to guess their meanings.

Signal, negative, correct, graph, figure, original, fundamental, experiment, mechanical, engineering, examination, polarity, specify, effective, voltage, basic, denominator, stable, component, electronics, resistor, sine, form, amplitude.

II. a) Listen, repeat and memorize the following words and word-combinations. b) Check if you know their meanings.

negative feedback отрицательная обратная связь; index finger указательный палец; open-loop gain коэффициент усиления при разомкнутом контуре обратной связи; *A* closed-loop gain коэффициент

усиления при замкнутом контуре обратной связи; β feedback fraction коэффициент (передачи цепи) обратной связи; internal stray capacitance внутренняя паразитная емкость; excessive variation излишнее изменение; frequency response частотная характеристика; deficiency недостаток; frequency distortion частотное искажение; plot v. изображать, наносить данные на график; flatten v. сглаживать; ruler up понижение; overall loss общая потеря; touch at the tips касаться кончиками; to control the speed of rotating machinery управлять скоростью вращения машины; be accurately predictable быть точно предсказуемым; make clear the effect выяснить влияние; feedback loop incorporating an attenuator which feeds a fixed fraction цепь (петля) обратной связи, содержащая аттенюатор, который передает определенную часть; enormous fall in gain at high frequencies большое падение коэффициента усиления на высоких частотах.

III. a) Analyse the constituents the following words consist of. b) Translate these words into Russian.

Amplifier, largely, capacitance, excessive, variation, distortion, feedback, greater, equation, independent, capacitor, probably, governor, rotating, calculation, simply, input, output, rearranging, equation, closed-loop, immediately, situation, exactly, subtracting, adding, independent, precisely.

IV. Repeat these formulas after the speaker and learn their reading.

$A = \frac{U_{out}}{U_{in}}$ *A* is equal to *U* sub out divided by *U* sub in.

$e = U_{in} + \beta U_{out}$ *e* is equal to *U* sub in plus β multiplied by *U* sub out.

$U_{out} = A_0(U_{in} + \beta U_{out})$ *U* sub out is equal to *A* sub 0 round bracket open *U* sub in plus β multiplied by *U* sub out round bracket closed.

$\beta A_0 \gg 1$ β multiplied by A_0 larger than one.

$A \approx \frac{A_0}{\beta A_0}$ *A* approximately equal to *A* sub 0 divided by β multiplied by *A* sub 0.

Text A

FREQUENCY RESPONSE

I. a) Listen to the text, mind the English intonation. b) Read the text to yourself and grasp the main idea of it.

No amplifier gives the same gain at all frequencies. The gain of any amplifier begins to fall at high frequencies largely as a result of its internal stray capacitance. When an amplifier exhibits excessive variation of gain with signal frequency, it is said to have a poor frequency response. This deficiency is sometimes referred to as frequency distortion, but must not be confused with non-linear distortion. Negative feedback can correct a poor frequency response as long as the

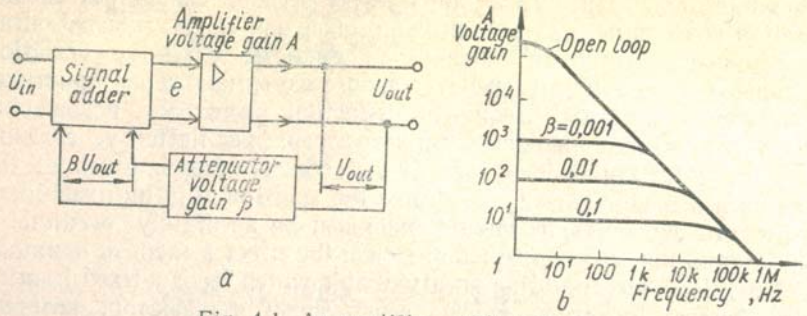

Fig. 4.1. An amplifier with feedback:
a functional diagram; *b* frequency response with different feedback factors.

open-loop gain remains greater than the closed-loop gain. Fig. 4.1*b* shows the graphs of the gain of an amplifier plotted against frequency. The top line shows the open-loop gain; the enormous fall in gain at high frequencies is in fact deliberately introduces by an internal capacitor for stability reasons. The lower curve illustrate the way that negative feedback flattens the frequency response but at the expense of gain; frequency responses are plotted for closed-loop gains of 1000, 100 and 10 and are so level that they can be drawn with a ruler up to the region where the closed-loop gain approaches the open-loop figure.

Although the overall loss of gain with negative feedback may appear serious, it is in fact easy to connect two negative feed-back amplifier in cascade (i. e. one after the other) and thus return to a gain figure similar to the original open-loop gain but with a much improved frequency response.

2. Average Reading

Text B

EQUATION FOR AN AMPLIFIER WITH FEEDBACK

I. a) Listen to the text. b) Read it (time limit is 5 min.). c) Find the part of it dealing with a block diagram of an amplifier of voltage gain A_0 with a feedback loop. Translate it.

The concept of negative feedback is fundamental to life. A simple experiment will illustrate this point: close your eyes and then bring your index fingers together so that they touch at the tips. You will probably miss.

Examples of negative feedback can also be found in the field of mechanical engineering. One of the clearest examples is the governor which is used to control the speed of rotating machinery.

An examination of a basic feedback circuit together with one or two simple calculations will make clear the effect of negative feedback. Fig. 4.1*a* is a block diagram of an amplifier of voltage gain A_0 with a feedback loop incorporating an attenuator which feeds a fixed fraction, β, of the output back to the input. In this case, we shall

keep the polarity of amplifier gain and feedback positive, the feedback signal added to the input signal.

In Fig. 4.1*a* we can specify the effective voltage gain, A, of the amplifier with feedback. This is given simply by the ratio of the output voltage to input voltage, $A = \frac{U_{out}}{U_{in}}$. Now we shall consider the signal e at the input of the basic amplifier of gain A_0: $e = U_{in} + \beta U_{out}$, also, we know $U_{out} = A_0 e$, therefore $U_{out} = A_0 (U_{in} + \beta U_{out})$. Rearranging, $U_{out}(1 - \beta A_0) = A_0 U_{in}$, hence

$$A = \frac{U_{out}}{U_{in}} = \frac{A_0}{1 - \beta A_0}. \qquad (4.1)$$

Equation (4.1) is the general equation for an amplifier with feedback. The basic gain, A_0, is often referred to as the open-loop gain and the gain with feedback, A, as the closed-loop gain. The feedback is positive and it may be seen immediately that when $\beta A_0 = 1$, an interesting situation develops in that A becomes infinite. Infinite gain implies that the amplifier will give an output signal with no input, and this is exactly what happens. Positive feedback is the bases of oscillators (signal generators).

For negative feedback, we can make β negative by subtracting the feedback from the input instead of adding.

Then
$$A = \frac{A_0}{1 + \beta A_0}. \qquad (4.2)$$

Now if, as is usually the case, $\beta A_0 \gg 1$ then we can neglect the 1 in the denominator and

$$A \approx \frac{A_0}{\beta A_0}, \text{ i. e. } A \approx \frac{1}{\beta}. \qquad (4.3)$$

This is the most significant equation because, for the first time, we have "designed" an amplifier with a precisely determined voltage gain. As long as the open-loop gain is much larger than the closed-loop gain (e. g. a hundred times greater) then the closed-loop gain is independent of the amplifier characteristics and dependent only on β. This feedback fraction, β, usually depends upon just two resistors in a potential divider. Resistors are the most stable components in electronics; their value can be precisely specified to any desired accuracy and is unlikely to change with time. Negative feedback extends these attributes of accuracy and stability to the gain of the entire amplifier.

ASSIGNMENTS

I. a) Choose the key sentences from the Text A and compare them with the title of the text. b) Say what the text is about.

II. Skim through the Text B and find the part of it dealing with the general equation for an amplifier with feedback.

III. Find the part in the Text B containing information about resistors as the most stable components in electronics. Translate it.

IV. Answer the following questions embracing the contents of the Text A and the Text B.

1. What is the concept of negative feedback? 2. What experiment may illustrate the concept of negative feedback? 3. Where can examples of negative feedback be found? 4. Where can examples of closed-loop gain be found? 5. What makes clear the effect of negative feedback? 6. What is shown in Fig. 4.1*a*? 7. What feedback is the basis of oscillators?

V. Translate the following word-combinations into English and memorize their English equivalents.

Фактически; легко соединить; одним из ярких примеров; в общем случае; обычно зависит от; это расширяет понятие.

VI. Prepare a dialogue on an amplifier with the feedback (Fig. 4.1*a*)

VII. Examine Fig. 4.1*b* and comment on frequence response with different feedback factors.

VIII. Speak on negative feedback of an amplifier.

IX. Retell the Text B according to your own plan.

X. Make a short written summary of the Text A and the Text B.

II. CLASSWORK

3. Close Reading

PRE-TEXT EXERCISES

I. Be sure that you know these words and word-combinations.

Occur встречаться; virtually фактически, в сущности; well worth trading можно легко обменять; version вариант; drop падать; excursion отклонение, уход; unwanted addition нежелательное дополнение; in order to maintain для того, чтобы поддержать; boost v. повышать; in return в свою очередь.

II. Find these word-combinations in the Text C and translate the sentences containing them.

Perfect magnified replica совершенная (идеальная) усиленная копия; clipping distortion искажение за счет ограничения; pointless exercise бессмысленное упражнение; boost v. усиливать.

Text C

NON-LINEAR DISTORTION

I. a) Read the text. b) Speak on the variaties of distortion.

Distortion occurs when an amplifier does not present a perfect magnified replica of the input wave form but changes its shape in some way because of a non-linear transfer characteristic. Fig. 4.2 shows a pure sine wave together with two versions of the same waveform after it has been subjected to different forms of non-linear distortion. These varieties of distortion arise because the gain of the amplifier is in some way dependent upon the instantaneous signal amplitude. In Fig. 4.2*b* the amplifier gain is dropping at large positive or negative signal excursion ("clipping distortion"), whilst in Fig. 4.2*c* it is when the signal is very low in amplitude, near the zero crossing, that the gain falls.

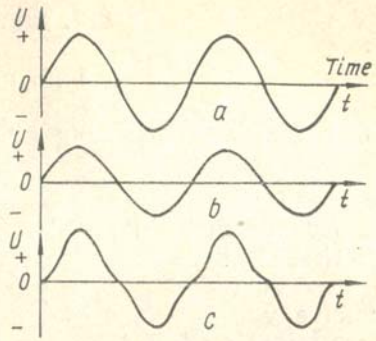

Fig. 4.2. The waveforms in amplifier circuits:
a pure sine wave; *b* clipping distortion: *c* crossover distortion.

Non-linear distortion can be seen as an unwanted addition by the amplifier to the original signal. When negative feedback is applied to an amplifier, distortion is reduced by the factor $(1 + A_0)$ but, in return, the input signal must be increased by the factor $(1 + A_0)$ in order to maintain the output signal.

The use of a second amplifier to boost the input by the factor $(1 + A_0)$ need not significantly contribute to the total distortion since only small signals are being handled at that stage of the processing. Voltage gain is cheap and well worth trading for low distortion. It is difficult to design a power amplifier with less than 1 % total harmonic distortion under open-loop conditions, but with negative feedback figures lower than 0.1 % are common in high-quality audio amplifiers.

ASSIGNMENTS

I. Divide the text into logical parts. Entitle each part.

II. Find the part in the text containing information about non-linear distortion. Translate it.

III. Answer the following questions embracing the contents of the Text C.

1. When does distortion occur? 2. What does Fig. 4.2 show? 3. Why do these varieties of distortion arise? 4. Is the amplifier gain in Fig. 4.2*b* dropping at large positive or negative signal excursion? 5. How can non-linear distortion be seen? 6. Is it difficult to design a power amplifier with less than 1 % total harmonic distortion?

IV. Ask additional questions on the Text C.

V. Combine your answers into a short summary of the text.

VI. Speak on:

1. Non-linear distortion.
2. Voltage gain.

VII. Examine Fig. 4.2 and comment on:

1. Pure sine wave.
2. Clipping distortion.
3. Crossover distortion.

VIII. Find the sentences in the Text C with the verbs in the Continuous and Perfect Tense. Translate them.

IX. Translate the Text C to be sure you understand it well.

4. Searching Reading

PRE-TEXT EXERCISES

I. Match the following English words and word-combinations with the Russian ones.

impedance	удобный метод
impedance matching	неизбежно
at first sight	сводится
assess v.	полное сопротивление, импеданс
resolve v.	на этом этапе
convenient method	уместно отметить
in the way	в последовательной цепи (по пути)
invariably	удобное представление
it is relevant to point out	подтверждать
confirm	согласование сопротивлений
at this stage	на первый взгляд
convenient representation	представить в виде

II. Pick out all technical terms from the Text D and translate sentences with them.

III. Translate the following word-combinations from the text.

Any electrical device; just like any other impedance; at first sight; however complicated; in the majority of circuits; in such cases; it is important to note.

Text D

INPUT AND OUTPUT IMPEDANCES

I. Read the text and say about the input impedance of a circuit such as a bipolar transistor amplifier.

Any electrical device which requires a signal for its operation has an input impedance. Just like any other impedance (or resistance in d. c. circuit), the input impedance of a device is a measure of the current drawn by the input with a certain voltage across it.

The input impedance of a circuit such as a bipolar transistor amplifier might seem to be more complicated. At first sight, the presence of capacitors, resistors and semiconductor junction in a circuit makes the input impedance difficult to assess. However, any input circuit, however complicated, may be resolved into the simple impedance shown in Fig. 4.3*a*. If U_{in} is the a. c. input signal voltage and I_{in} the a. c. current drawn by the input, then input impedance

$$Z_{in} = \frac{U_{in}}{I_{in}}. \qquad (4.4)$$

In the majority of circuits, the input impedance is resistive over most of the frequency range, there being negligible phase difference between input voltage and input current. In such cases, the input appears as the circuit of Fig. 4.3b and Ohm's law applies, the complex algebra

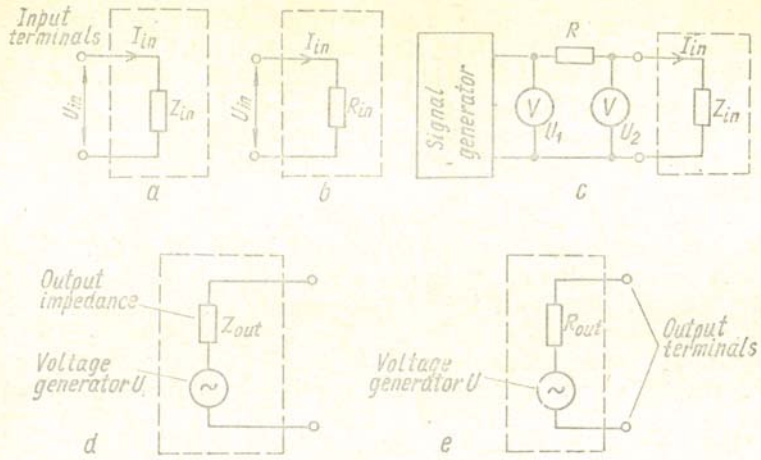

Fig. 4.3. Input and output impedances:
a a pair of input terminals with input impedances Z_{in}; *b* a device with a resistive input impedance; *c* a circuit for input impedance measurement; *d* Thevenin's equivalent circuit, applicable to any pair of output terminals; *e* an equivalent circuit applicable to devices with resistive output impedance.

and vector diagrams of reactive circuits being unnecessary. It is important to note, however, that a resistive input impedance does not necessarily mean that a d. c. signal can be used to measure the input resistance; there may be reactive components in the way (e. g. a coupling capacitor) which, whilst insignificant at moderate a. c. frequencies will prevent d. c. measurement from being made on the input. The most convenient method for input impedance measurement is shown in the circuit of Fig. 4.3*c*.

All output circuits, both a. c. and d. c. invariably have a certain output impedance associated with a voltage generator. That this simple description applies to even the most complicated circuits is confirmed by Thevenin's theorem, which states: any network of impedance and generators having two output terminals may be replaced by the series combinations of one impedance and one generator. Here, a "generator" is assumed to be an ideal voltage-producing device which continue to produce a constant voltage even when current is drawn from it. Thevenin's description of an output circuit is shown in Fig. 4.3*d*, Z_{out} being the output impedance and U the open-circuit output voltage.

ASSIGNMENTS

I. Answer the following questions embracing the contents of the Text D.

1. What device has an input impedance? 2. What is shown in Fig. 4.3*a*? 3. What is the input impedance in the majority of circuits? 4. What makes the input impedance difficult to assess? 5. What is the input impedance? 6. What means a resistive input impedance? 7. What is the output impedance? 8. What does Thevenin's theorem state?

9. Where is Thevenin's description of an output circuit shown?
10. What does the equivalent circuit represent in Fig. 4.3*e*?

II. Discuss the problem of input and output impedances.

III. Prepare a dialogue on:

1. A device with a resistive input impedance.
2. An equivalent circuit applicable to most devices: resistive output impedance.

IV. Examine Fig. 4.3 and comment on:

1. A pair of input terminals with input impedances Z_{in}.
2. A device with a resistive input impedance.
3. A circuit for input impedance measurement.

V. Speak on:

1. Input impedance.
2. Thevenin's equivalent circuit, applicable to any pair of output terminals.

VI. Express your opinion of negative feedback.

VII. Look through the latest magazines, find additional material on he topic and discuss it with your fellow-students.

III. GRAMMAR EXERCISES

I. Analyse the structure of the following sentences. Translate them.

1. Negative feedback can correct a poor frequency as long as the open-loop gain remains greater than the closed-loop gain. 2. The lower curves illustrate the way that negative feedback flattens the frequency response but at the expense of gain; frequency responses are plotted for closed loop gains of 1000, 100 and 10 and are so leveled that they can be drawn with a ruler up to the region where the closed-loop gain approaches the open-loop figure. 3. Infinite gain implies that the amplifier will give an output signal with no input, and this is exactly what happens. 4. Distortion occurs when an amplifier does not present a perfect magnified replica of the input wave form but changes its shape in some way because of a non-linear transfer characteristics.

II. Define the function of the Infinitive in these sentences and translate them.

1. The input impedance of a circuit such as a bipolar transistor amplifier might seem to be more complicated. 2. When an amplifier exhibits excessive variation of gain with signal frequency, it is said to have a poor frequency response. 3. One of the clearest example is the governor which is used to control the speed of rotating machinery. 4. Here, a "generator" is assumed to be an ideal voltage-producing device which continue to produce a constant voltage even when current is drawn from it.

III. Check if you know the Participle Complexes and translate the sentences with them.

1. In the majority of circuits, the input impedance is resistive over most of the frequency range, there being negligible phase difference between input voltage and the input current. 2. In such cases, the input appears as the circuit of Fig. 4.3 and Ohm's law applies, the

complex algebra and vector diagrams of reactive circuits being unnecessary. 3. In this case we shall keep the polarity of amplifier gain and feedback positive, the feedback signal being added to the input signal.

Lesson 2. THE EMITTER FOLLOWER AND THE DIRECT-COUPLED AMPLIFIER

I. INDEPENDENT WORK

In the Laboratory

1. Skimming Reading

PRE-TEXT EXERCISES

I. a) Make sure that you know these words. Say what Russian words help you to guess their meanings. b) Repeat these words after the speaker.

Transform, problem, emitter, signal, maximum, voltage, base, normally, potential, balanced, collector, paradox, identical, differential, voltmeter.

II. Check if you know the meanings of these words and word-combinations.

Emitter follower эмиттерный повторитель; straight прямо, непосредственно; feed v. питать(ся); to be fed вводиться, подаваться; supply rail шина питания; preferred value предпочтительная величина; step down the voltage понижать напряжение; as far as the signals are concerned по отношению к рассматриваемым сигналам; output signal swing capability способность выходного сигнала изменяться;

a. c. view of circuit тип схемы для переменного тока; in dotted form пунктиром; as distinct from в отличие от.

III. a) Give initial forms of the following words and define the function of suffixes. b) Translate these words.

Impedance, transformer, reducing, solution, condition, capability, assuming, reasonably, showing, slightly.

Text A

OUTPUT IMPEDANCE AND EMITTER FOLLOWER

I. a) Listen to the text, mind the English intonation. b) Read the text to yourself and grasp the main idea of it.

If an output impedance is to be reduced for the purpose of optimum voltage transfer to the next circuit, then a transformer will be of little advantage, for, in reducing the output impedance, it will also step down the voltage. A much more satisfactory solution to the problem is the use of a transistor in the emitter follower (common collector) circuit. In this circuit the voltage gain is just a little less than unity. However, because the transistor gives a current gain, the emitter follower lowers the output impedance of any signal source connected to the input.

2. Average Reading

Text B

THE EMITTER FOLLOWER CIRCUIT

I. a) Listen to the text. b) Read it (time limit is 3 min.). c) Find the part of it dealing with the base bias resistor.

The emitter follower circuit is shown in Fig. 4.4*a*. The emitter follower circuit is also named "common-collector". As the name "common-collector" suggests, the transistor collector is connected straight to the supply line which, as far as the signals are concerned, is the same thing as the earth (common) rail, because power supply outputs are always designed to present a very low impedance to signals. The output load resistor, R_L is in the emitter circuit, whilst the input signal is fed in between base and earth in the usual way.

Before we consider the behaviour of a. c. signals in the emitter follower, it is appropriate to consider d. c. quiescent (no signal) conditions. We must ensure that output signal is able to swing both positively (towards supply rail) or negatively (towards earth). For maximum output swing capability the quiescent emitter voltage should be midway between earth and supply, i. e. at about 4.5V in this example.

The base bias resistor, R_B, feeds sufficient base current into the base-emitter junction to maintain the required emitter current. In this example, we have assumed a value of 200 for the d. c. current gain h_{FE}. Thus, a 1 mA emitter current requires 1/200 mA base current

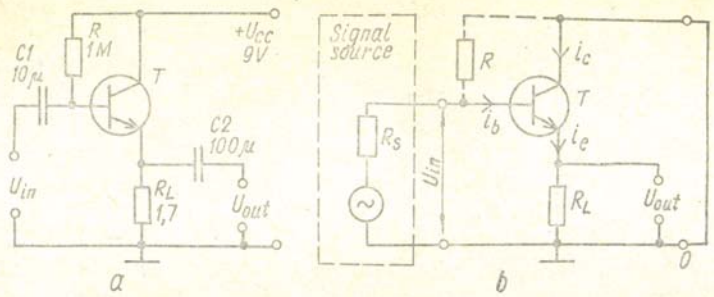

Fig. 4.4. The emitter follower:
a a simple circuit with typical parameters; *b* the circuit for a. c. signals.

(5 μ *A*) to maintain it. This current is provided by R_B whose value is calculated from Ohm's law, assuming the base voltage to be similar to the emitter voltage (4.5V). Voltage $R_B \cong (9 - 4{,}5)$ V; current in $R_B = 5 \cdot 10^{-6}$ A then,

$$R_B = \frac{9 - 4{,}5}{5 \cdot 10^{-6}}\,\Omega, \quad R_B = 900\,\text{k}\Omega.$$

A value of 1 mΩ is selected as a preferred value reasonably near to the calculated value.

To look at the behaviour of the a. c. signals, we shall redraw the circuit showing only these elements which are significant as far as the a. c. signals are concerned. This a. c. view of the circuit is in Fig. 4.4 *b*. Bias resistor R_B is shown in dotted form because we shall consider its effect only after we have followed the signal through the transistor. The connection between U_{CC} and earth indicates that, as far as the a. c. signal is concerned, the supply appears as a short circuit. Across the load, R_L is developed the output voltage signal U_{out}. These a. c. signal voltages and currents, are normally denoted by the lower case u and i as distinct from the upper case U and I which refer to d. c. voltage and current. We can see in Fig. 4.4 *b* that r_e and R_L constitute a potential divider for the signals, so that voltage gain A_U always turn out slightly less than unity:

$$A_U = \frac{R_L}{R_L + r_e}.$$

In this example, $R_L \cong 5\,\text{k}\Omega$ and $r_e \cong 25\,\Omega$, then

$$A_U = \frac{5000}{5000 + 25} = 0.995.$$

With the voltage gain so close to unity, the emitter voltage follows the base voltage very closely indeed, this action giving its name to the circuit.

ASSIGNMENTS

I. a) Choose the key sentences from the Text A and compare them with the title of the text. b) Say what the text is about.

II. a) Skim through the Text B and explain how the base bias resistor, R_B, feeds sufficient base current into the base-emitter junction.

III. Answer the following questions embracing the contents of the Text A and the Text B.

1. What is the voltage gain in the circuit shown in Fig. 4.4*a*? 2. Why does the emitter follower lower the output impedance of any signal source connected to the input? 3. Where is the output load resistor R_L? 4. What is the function of the base bias resistor? 5. What base current does a 1 mA emitter current require to maintain it? 6. How is the bias resistor chosen in Fig. 4.4*a*? 7. What does the connection between U_{CC} and earth indicate?

IV. Discuss the information obtained from the Text A and the Text B.

V. Be ready to discuss the information received at your lectures on speciality.

VI. Prepare a dialogue on a. c. signals in the emitter follower.

VII. Speak on the emitter follower as seen by a. c. signal.

VIII. Make short summaries of the Text A and the Text B.

II. CLASSWORK

3. Close Reading

PRE-TEXT EXERCISES

I. Be sure that you know these words.

Shift v. сдвигать, смещать; midway на полпути, посередине; interpose v. вставлять, входить между чем-л.; restrict ограничивать; earth земля; quiescent находящийся в покое, неподвижный; by means of посредством; with respect to по отношению к; further дальнейший; exhibit v. представлять.

II. Find the following word-combinations in the Text C and translate the sentences with them.

Coupling capacitor конденсатор связи; supply rail шина питания; permissible circuit voltage возможное (допускаемое) в цепи (схеме) напряжение; balanced power supply балансный источник питания; offset null control управление нулем сдвига; level-shifting arrangement устройство сдвига уровня.

III. Analyse the structure of these words and translate them.

Coupling, permissible, midway, two-transistor, complementary, consisting, slightly, divider, variable, zero-set, voltmeter, pointer.

IV. Find the English equivalents of the following word-combinations in the Text C.

В особенности; это, конечно, означает, что; в случае чего-л., посредством (с помощью); таким образом; с внешней стороны;

мы знаем, что; этот парадокс разрешается; оптимальное рабочее условие получается, когда; более чем.

Text C

DIRECT-COUPLED AMPLIFIER

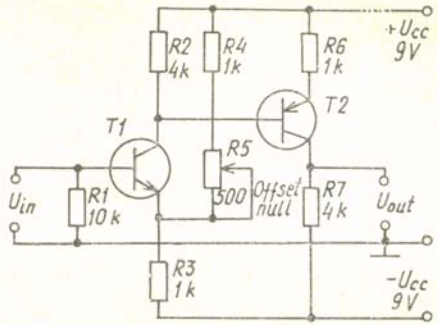

Fig 4.5. A simple d. c. amplifier.

I. a) Read the text. b) Find the part of it describing the optimum working condition obtained when T_2 quiescent collector potential is at earth (0V).

The design of an amplifier without coupling capacitors restricts the range of permissible circuit voltages. In particular, it is very desirable that, when there is no signal, both the input and the output should be at earth potential. This, of cause, means that the quiescent d. c. output voltage can no longer be set midway between earth (0V) and supply rail (U_{CC}). The solution in the case of the d. c. amplifier is to use two balanced power supplies, one positive and one negative.

A simple two-transistor d. c. amplifier is shown in Fig. 4.5. It uses balanced power supplies and complementary (n-p-n and p-n-p) transistors. By means of the potential divider, consisting of R_4 and R_5 with R_2, the emitter of T_1 is held at a potential just a slightly negative of earth (—0,6 V). Thus T_1 is correctly biased if its base is tied to earth via the input resistor R_1.

On the output side, we know that the collector of an n-p-n transistor must be positive with respect to the base and yet in this d. c. amplifier, we require the collector to be at earth potential if zero input is to give zero output. This paradox is resolved by T_2, a p-n-p transistor, which is interposed to shift the quiescent output voltage back to zero and at the same time to perform further amplification. T_2 is simply a fully-stabilized amplifier stage working between supplies of +9 V and —9 V, with its base potential held, not by a potential divider, but by T_1 collector. The optimum working condition is obtained when T_2 quiescent collector potential is at earth (0V), giving zero output voltage for zero input to T_1. If zero does not result in zero d. c. output, the amplifier is said to exhibit an offset voltage; the purpose of variable resistor R_5, "the offset null control" is to adjust for zero output with zero input, rather as a voltmeter zero-set screw is adjusted to bring the pointer to scale zero with no applied signal.

ASSIGNMENTS

I. Skim through the Text C and give the main idea of it.

II. a) Divide the text into logical parts. b) Choose the key sentences, analyse and translate them.

III. Comment on the author's attitude to direct-coupled amplifier.